REMARKS

This is in response to the Office Action of 03 February 2004. Claims 1-15, are pending in the application, and Claims 1-15 have been rejected.

By this Response, arguments traversing the rejections of Claims 1-15 are presented.

No new matter has been added.

In view of the remarks below, Applicants respectfully request reconsideration and further examination.

About The Invention

The present invention relates generally to methods and apparatus for accessing memory in a secure manner from both a wired and wireless interface.

Priority Documents

Applicants thank the Examiner for acknowledging receipt of all of the certified copies of the priority documents.

Information Disclosure Citation Form PTO-1449

Applicants thank the Examiner for returning an initialed and dated copy of Applicants' previously submitted Information Disclosure Citation form.

Rejections under 35 USC 102(e)

Claims 1-2, 6-8, and 12-13 have been rejected under 35 USC 102 (e) as being anticipated by Reiner, et al., (US Patent 5,875,450).

For at least the reasons set forth below, Applicants respectfully traverse the rejections under 35 USC 102(e), and request that these rejections be

withdrawn.

Reiner, et al., disclose a device for processing and storing data, in particular a chip card, that includes a first interface with contacts and a second contactless interface; a first controllable switching device that is operable to selectively connect either the first interface or the second interface to a memory by way of address, data, and control lines; a logic circuit that drives the first controllable switching device; a second controllable switching device disposed between the first switching device and the memory, the second controllable switching device being driven by the logic circuit and by an address signal present on the address lines. In other words, Reiner, et al., disclose a contacted interface and a contactless interface, each of which obtains address, data, and control signals from the devices to which they are respectively interfaced, and the two interfaces supply these respective address, data, and control signals to a multiplexer (i.e., first controllable switching device 3) that selects which set of address, data, and control signals are passed through to the memory. Reiner, et al., additionally disclose a second multiplexer (i.e., second controllable switching device 7) that receives the output of the first multiplexer, and either passes these signals to the memory, or which may "interrupt connection lines between the first controllable switching device 3 and the semiconductor memory 5" (col. 4, lines 54 through col. 5, line 2).

With respect to Applicants' independent Claims 1 and 7, a structure different than that disclosed by Reiner, et al., is recited. Reiner, et al., disclose a first and a second controllable switching device arranged in series, with a memory coupled to the second switching device, and each of a first and a second communication interface coupled to the first switching device. The structure defined by Applicant's Claim 1 is different from Reiner, et al., in at least the following the ways. First, the claimed structure does not have the series connected switchable devices of Reiner, et al. Rather, Claim 1 recites that (a) a first memory access means is between the first interface and the memory, and wherein only the first memory access device can access a first storage location in the memory; (b) a second memory access device is between the second

interface and the memory; and (c) an additional memory access device provides access to the first memory location for the second interface via the first memory access means. This additional memory access device, and the circuit pathway from the first storage location, through the first memory access device, the additional memory access device, the second memory access device, and finally to the second interface, is not disclosed, suggested, or motivated by the disclosure of Reiner, et al.

With respect to Applicants' independent Claim 13, a method different than that disclosed by Reiner, et al., is recited. Referring to the above discussion of the differences between the structure disclosed by Reiner, et al., and Applicants' claimed structure, it can be seen that the method of memory access with Applicants' structure is different that the method of memory access disclosed by Reiner, et al. More particularly, Claim 13 recites the access of a first memory location being possible only through the first memory access means (which is connected between the first interface and the memory), and that to access to the first memory location for the second interface, a pathway is established from the second interface through the second memory access means, through the additional memory access means, through the first memory access means, and finally to the memory itself. However, the second interface accesses the memory outside the first storage location by way of the much shorter pathway through only the second memory access means. Neither the additional memory access device (38) itself, nor establishing the pathway through the additional memory access device are disclosed, suggested, or motivated by the disclosure of Reiner, et al.

In view of the foregoing, Applicants respectfully submit that the rejection of independent Claims 1, 7 and 13, under 35 USC 102(e) should be withdrawn. Similarly, the rejection of dependent Claims 2, 6, 8 and 12, should also be withdrawn.

Rejections under 35 USC 103(a)

Claims 3, 5, 9, 11, and 14-15 have been rejected under 35 USC 103(a) as being unpatentable over Reiner, et al. Claims 4 and 10 have been rejected under 35 USC 103(a) as being unpatentable over Reiner, et al., in view of Schwarz, et al., (US Patent 5,675,645).

For at least the reasons set forth below, Applicants respectfully traverse the rejection of Claims 3-5, 9-11, and 14-15 under 35 USC 103(a) and request that these rejections be withdrawn.

Referring to the detailed discussions above with respect to independent Claims 1, 7, and 13, Applicants respectfully submit that Reiner, et al., do not disclose, suggest, or provide motivation for the recited limitations of the base Claims for Claims 3-5, 9-11, and 14-15. Applicants note that Reiner, et al., do not disclose or suggest either (a) the claimed structural arrangement, which includes the additional memory access means (38), or (b) the claimed method of providing memory access to the second interface by creating a pathway to the memory through the second memory access means, the additional memory access means, and the first memory access means. The fact the both Reiner, et al., and various ones of Applicants' dependent Claims relate to verification for memory access, does not make these dependent Claims unpatentable, because neither Reiner, et al., nor Schwarz, et al., whether taken singularly or in combination, produce the invention defined by Applicants' Claims.

Since the references do not disclose, suggest, or provide motivation for the invention defined by Claims 3-5, 9-11, and 14-15, Applicants respectfully submit that these rejections should be withdrawn.

Conclusion

All of the rejections in the outstanding Office Action of 03 February 2004 have been responded to, and Applicants respectfully submit that the pending

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Claims 1-15 are now in condition for allowance.

Applicants respectfully request that a timely Notice of Allowance be issued in this case.

Respectfully submitted,

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